Fault-Tolerant Operation of DFIG-WT with Four-Switch Three-Phase Grid-Side Converter by Using Simplified SVPWM Technique and Compensation Schemes

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***Abstract* -- In this paper, in response to the open-circuit fault scenario in the grid-side converter (GSC) of doubly-fed induction generator-based wind turbines (DFIG-WTs), a fault-tolerant four-switch three-phase (FSTP) topology-based GSC is studied. Compared with other switch-level fault-tolerant converter topologies, fewer switches, less switching and conduction losses, and simpler converter structure are derived. A simplified space vector pulse width modulation (SVPWM) technique is proposed to improve the output current quality and reduce the computational complexity in the control process. Unified expressions of duty ratios for the two remaining healthy bridge arms are obtained. In addition, a DC-bus voltage deviation suppression strategy is proposed to maximize the DC-bus voltage utilization rate and mitigate the damage to the DC-link capacitors. Furthermore, the three-phase unbalance phenomenon caused by the capacitive impedance in the faulty phase is analysed from the AC point of view, and a current distortion compensation scheme is illustrated. Simulations are carried out in Matlab/Simulink2017a to demonstrate the validity of the proposed SVPWM technique and compensation schemes in FSTP GSC for a 1.5MW grid-connected DFIG-WT when different working conditions are considered.**

***Index Terms*-- grid-side converter, doubly-fed induction generator-based wind turbine, four-switch three-phase, space vector pulse width modulation, compensation schemes.**

I. Nomenclature

V, I	Constant values of voltage and current
v, e, i, φ	Instantaneous values of voltage, source voltage, current and flux
V_{dc}, V_{dc1}, V_{dc2}, V_o	DC-link voltage, upper and lower capacitor voltages, and output voltage
E_m, V_m, I_m	Amplitudes of the three-phase source voltages, converter voltages and currents
ϕ	Phase angle
ΔV	Voltage difference
L_m, L_{ls}, L_{lr}	Mutual inductance, stator leakage inductance and rotor leakage inductance
R, L, Z	Resistance, inductance and impedance
P, Q	Active and reactive power
d	Duty ratios
f_{NOM}	Nominal grid frequency
θ_s, θ_r	Grid voltage angle and rotor angle
ω	Angular speed
ω_s	Synchronous angular frequency
T_m, T_e	Mechanical and electromagentic torque
T_s, T_{sw}	Sampling time and switching time
Subscripts & Superscripts	
s, r, t, g	Stator, rotor, total and grid-side values
a, b, c; A, B, C	Phases A, B, C; Points A, B, C
α, β; d, q	Direct and quadrature components referred to the stationary/synchronous reference frame
_ref; *_ref*1	Reference value; Transient DC reference value

II. Introduction

As one of the most important and promising renewable energy resources, wind energy attracted the attention of a number of researchers [1-3]. Since the doubly-fed induction generators (DFIGs) [4] are endowed with the characteristics of variable speed constant frequency (VSCF) operation, four-quadrant power regulation, and small volume based back-to-back power electronic converters, they are extremely eligible for wind power generation systems owing to the feature of wind speed fluctuation. However, most of DFIG-WTs are approaching the end of their service time [5], and faults are easy to occur in this case. According to [6], the semiconductor devices (power switches) in power converters are considered to be the most fragile components, and 21% of the faults in power converters are caused by the breakdown of these devices [7]. Once a switch breaks down to form an open circuit, a DFIG-WT has to disconnect from the grid. For offshore WTs [8, 9], which are developing fast in recent years, high maintenance cost and accessibility issues are inevitable. Therefore, it is necessary to increase the reliability of power electronic converters in DFIG-WTs to mitigate these deficiencies.

The fault-tolerant solutions proposed for switch-level faults can be generally categorized into [10] 1) inherently redundant switching states; 2) redundant parallel or series switches installation; 3) DC-bus midpoint connection. For the first two schemes, multiple switches are required, which complicates the circuit design process and leads to high switching losses. Therefore, the last option is chosen in this paper. In this topology, the faulty phase is connected to the midpoint of the DC bus. Then, the post-fault converter can still work normally with only four switches, and this fault-tolerant topology is named as four-switch three-phase (FSTP), with respect to its six-switch three-phase (SSTP) counterpart in the normal case. Since the number of switches is reduced, lower switching and conduction losses can be derived, and the circuit simplicity is achieved. However, several shortcomings are presented for FSTP topology. For example, the voltage gain is reduced, and the current rating increases if the output power is going to remain the same [11]. In addition, phase current distortion and unbalance are caused due to asymmetry among the three phases [12]. Moreover, the DC-bus voltage unbalance and fluctuation are induced as the current in the faulty phase flows through the centre tap of the two DC-link capacitors [13].

In order to improve the performance of FSTP converter, many relevant researches were carried out. The mathematical model of FSTP pulse width modulation (PWM) voltage source rectifier (VSR) was first derived in *dq* frame for control design purpose in [14]. The number of switching states is four for FSTP topology, instead of eight for an SSTP one, since only four switches are controllable under this situation, and no zero vector is intrinsically available. Due to this characteristic, different categories of space vector PWM (SVPWM) techniques were proposed for FSTP converters, where three or four [15] out of all the switching states can be applied for output voltage synthesis. In [15], a general PWM strategy was proposed for FSTP inverters. For the SVPWM techniques for FSTP converters, two basic voltage vectors in opposite directions with smaller amplitudes (SVSVM) [16], with larger amplitudes (LVSVM) [11, 17], and three nearest voltage vectors to the output one (NTSVM) [18] can be used to generate the equivalent zero voltage vectors. A control-oriented model for FSTP rectifier was built in *dq* synchronous reference frame under balanced voltage in [13], and it was concluded that the employment of SVSVM introduces the smallest current ripples. Moreover, hybrid SVPWM strategies were researched in [19, 20] for capacitor current stress reduction and torque ripple minimization. Furthermore, finite states model predictive control was investigated for bidirectional FSTP AC/DC converters under unbalanced grid voltages in [21] to achieve power compensation. While none of these strategies were demonstrated to be effective in grid-connected DFIG-WTs.

As the other competitive candidate for wind energy conversion systems (WECSs), permanent magnet synchronous generator (PMSG) is widely applied, and relevant investigations in fault-tolerant operation of the power converters with FSTP topology were carried out [22, 23]. However, sector identification is still required in the modulation process.

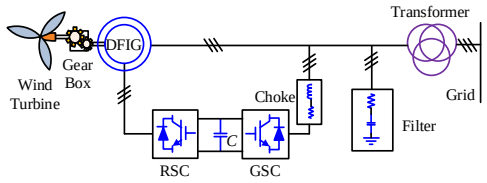


Fig. 1. Traditional configuration of DFIG-WT

The traditional configuration of DFIG-WT is shown in Fig. 1. The grid-side converter (GSC) is responsible for keeping a steady DC-bus voltage, maintaining sinusoidal three-phase grid currents, and regulating the power factor, and the functions of the rotor-side converter (RSC) are controlling the stator active and reactive power [24]. In [25], FSTP topologies were applied in both the GSC and RSC to realize the DFIG-WT system reconfiguration. However, the modulation technique was outdated. Therefore, a simplified SVPWM technique was proposed for the FSTP GSC of DFIG-WT to allow the post-fault system to continue working properly in [26], while only one working condition was included and no in-depth analysis for current distortion was presented. This paper is a continuous work of [26] and grid voltage sag is considered. In addition, the DC-link voltage deviation suppression scheme is explained in detail for maximizing the DC-bus voltage utilization rate. Moreover, the phase current distortion caused by DC-bus midpoint connection is illustrated from the aspect of source impedance unbalance, and the compensation scheme is applied to increase the overall quality of the three-phase grid currents.

The organization of this paper is as follows: In Section III, the *dq* dynamic modelling of DFIG-WT is briefly described. Then the fault-tolerant FSTP GSC topology is illustrated in Section IV, with the operational modes and current flows analysed. In Section V, the proposed simplified SVPWM is explained, and the unified expressions for duty ratios in the two healthy bridge arms are obtained. In addition, the current distortion caused by capacitive impedance in the faulty phase is illuminated in Section VI. In Section VII, the control strategy to be applied for FSTP GSC is illustrated. Afterwards, the simulation results and discussion are given in Section VIII. Finally, the conclusion is presented in Section IX.

III. Dynamic Modelling of DFIG-WT in *DQ* Synchronous Reference Frame

In order to emulate the method of model analysis in a DC motor, Clarke and Park transformations [27] are usually utilized in the dynamic modelling of DFIG. Grid voltage orientation (GVO) is applied owing to its simplicity in control, then the voltage equations of DFIG can be written as

$$\begin{cases} \vec{v}_s = R_s\vec{i}_s + \dfrac{d\vec{\varphi}_s}{dt} + j\omega_s\vec{\varphi}_s \\ \vec{v}_r = R_r\vec{i}_r + \dfrac{d\vec{\varphi}_r}{dt} + j\omega_{slip}\vec{\varphi}_r \end{cases} \tag{1}$$

where

$$\omega_{slip} = \omega_s - \omega_r \tag{2}$$

The flux equations, electromagnetic torque equation and the kinetic equation can be expressed respectively as

$$\begin{cases} \vec{\varphi}_s = L_s\vec{i}_s + L_m\vec{i}_r \\ \vec{\varphi}_r = L_m\vec{i}_s + L_r\vec{i}_r \end{cases} \tag{3}$$

$$T_e = n_p L_m(i_{rd}i_{sq} - i_{rq}i_{sd}) \tag{4}$$

$$T_e - T_L = \frac{J}{n_p}\frac{d\omega_r}{dt} \tag{5}$$

Setting up the dynamic model of DFIG-WT clarifies the relationships among the voltages, currents, fluxes and torques, which is of paramount importance in the control process.

IV. Fault-Tolerant FSTP GSC Topology for DFIG-WT

According to [28], the faulty cases in different bridge arms are identical essentially. Take the case that the open circuit occurs in the bridge arm connected to phase A in GSC, which is illustrated in Fig. 2.

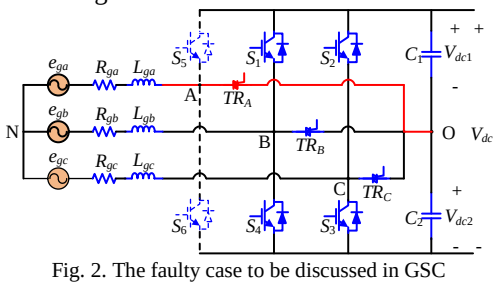


Fig. 2. The faulty case to be discussed in GSC

The DC-link capacitances are considered to be the same (C_1 = C_2 = C_{DC}). The three-phase grid circuit is assumed to be balanced ($R_{ga} = R_{gb} = R_{gc} = R$, $L_{ga} = L_{gb} = L_{gc} = L$). A triac ($TR_A$, TR_B, TR_C) is placed between the connecting point of each bridge arm (A, B or C) and the midpoint of the DC-bus (O). When the GSC operates in the normal case, six switches (S_1 to S_6) are applied for controlling the power flows. In this paper, S_5 or S_6 is assumed to break down, and only four switches (S_1 to S_4) are controllable under this circumstance. The post-fault FSTP topology is established by activating TR_A to connect phase A to the midpoint of DC-bus.

A. Operational Modes of DFIG

Since the power electronic converters are not used for energy conversion when DFIG operates in synchronous operational mode (slip = 0), only the cases with slip > 0 and slip < 0 (subsynchronous and supersynchronous respectively) are taken into consideration in this paper.

The switching functions S_a, S_b and S_c are defined to represent the switching states of the six switches when SSTP topology is applied. $S_a/S_b/S_c$ can be either 0 or 1 to indicate the situation that $S_5/S_1/S_2$ is turned off and $S_6/S_4/S_3$ is turned on, or vice versa. In the FSTP topology considered in this paper, only the switching functions S_b and S_c are used.

B. Current Flows in FSTP GSC

Assume that the DFIG-WT operates in the subsynchronous mode, then the current flows in FSTP GSC are illustrated in Fig. 3 for the four switching states (V_{00}, V_{10}, V_{11} and V_{01}). The expressions for i_{C1} and i_{C2} in this case are

$$\begin{cases} i_{C1} = S_b i_{gb} + S_c i_{gc} - i_r = C_{DC}\dfrac{dV_{dc1}}{dt} \\ i_{C2} = (S_b - 1) i_{gb} + (S_c - 1) i_{gc} - i_r = C_{DC}\dfrac{dV_{dc2}}{dt} \end{cases} \tag{6}$$

The current in phase A can be derived by subtracting i_{c1} from i_{c2}.

$$i_{ga} = i_{C2} - i_{C1} = C_{DC}\frac{d(V_{dc2} - V_{dc1})}{dt} \tag{7}$$

The voltage difference ΔV between the two DC-link capacitors can be derived by implementing integral on both sides of (7), which is shown below.

$$\Delta V = V_{dc2}(t) - V_{dc1}(t) = \frac{1}{C_{DC}}\int_0^t i_{ga}dt + V_{dc2}(0) - V_{dc1}(0) \tag{8}$$

The terms $V_{dc1}(0)$ and $V_{dc2}(0)$ are the initial values of V_{dc1} and V_{dc2}. If the DFIG-WT operates in the supersynchronous mode, the following equations are satisfied.

$$\begin{cases} i_{C1} = -S_b i_{gb} - S_c i_{gc} + i_r = C_{DC}\dfrac{dV_{dc1}}{dt} \\ i_{C2} = (1 - S_b) i_{gb} + (1 - S_c) i_{gc} + i_r = C_{DC}\dfrac{dV_{dc2}}{dt} \end{cases} \tag{9}$$

$$i_{ga} = i_{C1} - i_{C2} = C_{DC}\frac{d(V_{dc1} - V_{dc2})}{dt} \tag{10}$$

$$\Delta V = V_{dc1}(t) - V_{dc2}(t) = \frac{1}{C_{DC}}\int_0^t i_{ga}dt + V_{dc1}(0) - V_{dc2}(0) \tag{11}$$

The values of three-phase GSC AC voltages are displayed in TABLE I.

TABLE I
THREE-PHASE GSC AC VOLTAGES

Vector	v_A	v_B	v_C	v_α	v_β
V_{00}	$\frac{2V_{dc2}}{3}$	$-\frac{V_{dc2}}{3}$	$-\frac{V_{dc2}}{3}$	$\frac{2V_{dc2}}{3}$	0
V_{10}	$\frac{V_{dc2}-V_{dc1}}{3}$	$\frac{2V_{dc1}+V_{dc2}}{3}$	$-\frac{V_{dc1}+2V_{dc2}}{3}$	$\frac{V_{dc2}-V_{dc1}}{3}$	$\frac{(V_{dc1}+V_{dc2})}{\sqrt{3}}$
V_{11}	$-\frac{2V_{dc1}}{3}$	$\frac{V_{dc1}}{3}$	$\frac{V_{dc1}}{3}$	$-\frac{2V_{dc1}}{3}$	0
V_{01}	$\frac{V_{dc2}-V_{dc1}}{3}$	$-\frac{V_{dc1}+2V_{dc2}}{3}$	$\frac{2V_{dc1}+V_{dc2}}{3}$	$\frac{V_{dc2}-V_{dc1}}{3}$	$\frac{(V_{dc1}+V_{dc2})}{\sqrt{3}}$

The expressions for v_A, v_B and v_C are then obtained as

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \frac{1}{3}\begin{bmatrix} -S_b - S_c & -S_b - S_c + 2 \\ 2S_b - S_c & 2S_b - S_c - 1 \\ -S_b + 2S_c & -S_b + 2S_c - 1 \end{bmatrix}\begin{bmatrix} V_{dc1} \\ V_{dc2} \end{bmatrix} \tag{12}$$

V. PROPOSED SVPWM TECHNIQUE FOR FSTP GSC

SVPWM technique is usually employed to synthesize the reference voltage vector, since it induces less current distortion compared to the conventional carrier-based PWM technique [29, 30]. In an FSTP converter, there is no intrinsic zero vector to be utilized. Therefore, it is necessary to create equivalent zero voltage vectors by applying the vectors with opposite components to obtain zero volt-second integral. However, when the converter operates with FSTP topology, the DC-bus utilization rate is much smaller than that for the SSTP case, which can be expressed as [11]

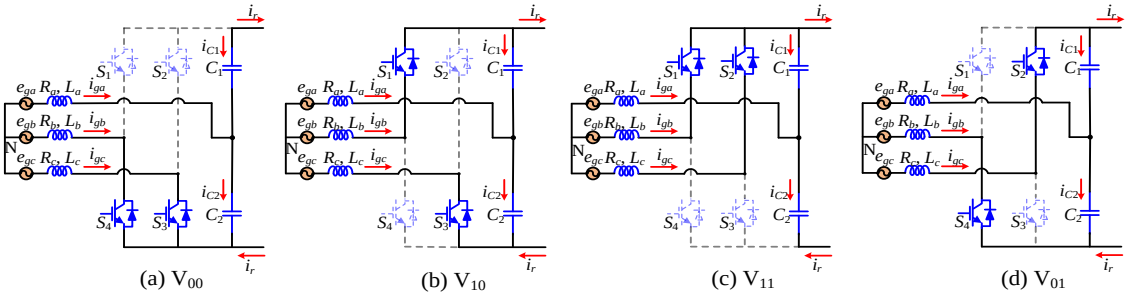
$$V_o = \begin{cases} V_{dc}/\sqrt{3} & \text{SSTP} \\ \min(V_{dc1}, V_{dc2})/\sqrt{3} & \text{FSTP} \end{cases} \tag{13}$$

A. SVPWM Techniques for SSTP and FSTP Topologies

If the voltages on the upper and lower DC-link capacitors C_1 and C_2 are equal ($0.5V_{dc}$), the maximum value of V_o is derived, which is $V_{dc}/(2\sqrt{3})$. On the other hand, if unbalance between V_{dc1} and V_{dc2} is presented, then: 1) When $V_{dc1} > V_{dc2}$, it takes longer time for capacitor C_1 to discharge, which increases the duration of V_{11}; 2) When $V_{dc1} < V_{dc2}$, it takes longer time for capacitor C_2 to discharge, which increases the duration of V_{00}. Therefore, the voltage utilization rate is further reduced. The space vector diagrams for SSTP and FSTP converters are illustrated in Fig. 4 for comparison.

The area of each circle in Fig. 4 intuitively describes the DC-bus voltage utilization rate for each case. OA, OB, OC and OD represent V_{00}, V_{10}, V_{11} and V_{01}, respectively. The blue rhombus is divided into four sectors. The smallest circle in Fig. 4 represents the DC-bus utilization rate in the case that $V_{dc1} < V_{dc2}$. In order to minimize the increase in the DC-bus voltage value while keeping the same active power output, balancing the DC-link capacitor voltages is significant.

It was found in [13] that lower current ripple is derived by using SVSVM. Therefore, in this paper SVSVM is applied, and the vectors in $\alpha\beta$ plane for FSTP topology are depicted in Fig. 5 assuming V_o is located in Sector I.



(a) V_{00} (b) V_{10} (c) V_{11} (d) V_{01}

Fig. 3. Current flows in FSTP GSC in subsynchronous operational mode for the four switching states

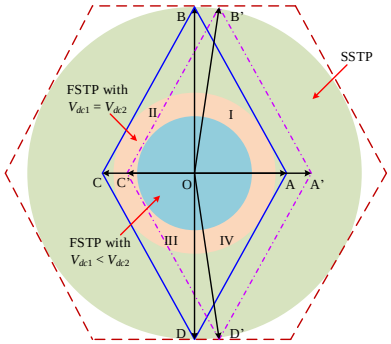


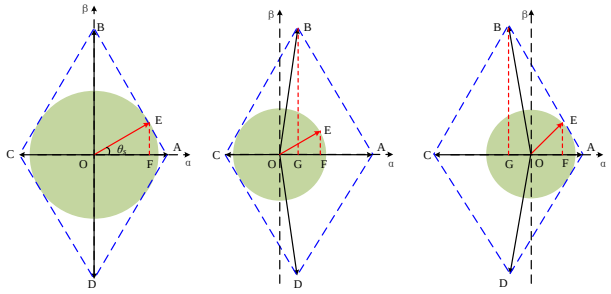
Fig. 4. Space vector diagrams for SSTP and FSTP converters

B. Proposed Simplified SVPWM Technique

The output voltage vector is represented by **OE**, and its projections on the α-axis and β-axis are denoted by **OF** and **FE** respectively. OF and EF can be obtained as

$$\mathrm{OF}=\begin{cases}\mathrm{OA}\times d_{00}-\mathrm{OC}\times d_{11} & V_{dc1}=V_{dc2}\\ \mathrm{OA}\times d_{00}-\mathrm{OC}\times d_{11}+\mathrm{OG}\times d_{10} & V_{dc1}<V_{dc2}\\ \mathrm{OA}\times d_{00}-\mathrm{OC}\times d_{11}-\mathrm{OG}\times d_{10} & V_{dc1}>V_{dc2}\end{cases} \tag{14}$$

$$\mathrm{EF}=\begin{cases}\mathrm{BO}\times d_{10} & V_{dc1}=V_{dc2}\\ \mathrm{BG}\times d_{10} & V_{dc1}\neq V_{dc2}\end{cases} \tag{15}$$



(a) $V_{dc1} = V_{dc2}$ (b) $V_{dc1} < V_{dc2}$ (c) $V_{dc1} > V_{dc2}$

Fig. 5. Space vector allocation for FSTP topology (OE in Sector I)

The values of OE, OF and EF can be expressed by

$$\begin{cases}\mathrm{OE}=V_m\\ \mathrm{OF}=v_{A\_ref}\\ \mathrm{EF}=\dfrac{v_{B\_ref}-v_{C\_ref}}{\sqrt{3}}\end{cases} \tag{16}$$

Also, the relationship among the duty ratios of the three switching states is

$$d_{00}+d_{10}+d_{11}=1 \tag{17}$$

According to equations (14) – (17) and the values of $\alpha\beta$ components for V_o in each switching state, the duty ratios for all the utilized switching states are calculated as

$$\begin{cases}d_{00}=\dfrac{V_{dc1}+v_{A\_ref}-v_{B\_ref}}{V_{dc}}\\ d_{10}=\dfrac{v_{B\_ref}-v_{C\_ref}}{V_{dc}}\\ d_{11}=\dfrac{V_{dc2}+v_{C\_ref}-v_{A\_ref}}{V_{dc}}\end{cases} \tag{18}$$

Then, the duty ratios for the bridge arms with (S_1, S_4) and (S_2, S_3) can be derived, which are represented as d_b and d_c

$$\begin{cases}d_b=d_{10}+d_{11}=\dfrac{V_{dc2}+v_{B\_ref}-v_{A\_ref}}{V_{dc}}\\ d_c=d_{11}=\dfrac{V_{dc2}+v_{C\_ref}-v_{A\_ref}}{V_{dc}}\end{cases} \tag{19}$$

The above equations are also applicable when V_o locates in other sectors, in which case there is no need to identify the sector. Therefore, complicated trigonometric calculations are eliminated to make the SVPWM technique simplified.

VI. Current Distortion Analysis

After the reconfiguration is done for GSC, the capacitive impedance is presented in phase A, resulting in phase current unbalance. From the AC point of view, the source impedance in phase A is $2C_{DC}$. The equivalent circuit of the AC source model for FSTP GSC is displayed in Fig. 6.

The source impedances $Z_{ga} = Z_{gb} = Z_{gc} = Z$. The sum of the three-phase grid currents is equal to zero, so

$$\frac{e_{ga}-v_A}{Z}+\frac{e_{gb}-v_B}{Z}+\frac{e_{gc}-v_C}{Z}=0 \tag{20}$$

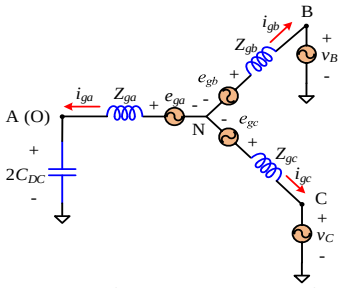


Fig. 6. Equivalent circuit of the AC source model for FSTP GSC in subsynchronous mode

The voltages at points B and C with respect to the DC-bus midpoint O can be obtained as

$$\begin{cases} v_{BO} = \sqrt{3}ZI_m \cos(\omega_s t + \phi - \frac{\pi}{6}) + e_{gb} - e_{ga} \\ v_{CO} = \sqrt{3}ZI_m \cos(\omega_s t + \phi + \frac{\pi}{6}) + e_{gc} - e_{ga} \end{cases} \quad (21)$$

According to Fig. 6, the three-phase GSC AC voltages can be expressed as

$$\begin{cases} v_A = i_{ga} / (j\omega_s 2C_{DC}) \\ v_B = e_{gb} - Zi_{gb} - e_{ga} + Zi_{ga} + v_A \\ v_C = e_{gc} - Zi_{gc} - e_{ga} + Zi_{ga} + v_A \end{cases} \quad (22)$$

With the condition $i_{ga} + i_{gb} + i_{gc} = 0$, the grid currents i_{gb} and i_{gc} are calculated as

$$\begin{cases} i_{gb} = \dfrac{3e_{gb} - 2v_B + v_C + v_A}{3Z} \\ i_{gc} = \dfrac{3e_{gc} - 2v_C + v_B + v_A}{3Z} \end{cases} \quad (23)$$

Then the expressions for the three-phase grid currents are achieved as

$$\begin{cases} i_{ga} = \dfrac{3Zj\omega_s C_{DC}}{1 + 3Zj\omega_s C_{DC}} I_m \cos(\omega_s t + \phi) \\ i_{gb} = I_m \cos(\omega_s t + \phi - \frac{2\pi}{3}) + \dfrac{i_{ga}}{6Zj\omega_s C_{DC}} \\ i_{gc} = I_m \cos(\omega_s t + \phi + \frac{2\pi}{3}) + \dfrac{i_{ga}}{6Zj\omega_s C_{DC}} \end{cases} \quad (24)$$

When the value of C_{DC} increases, the degree of current distortion is reduced. In addition, according to (11), the DC-link voltage unbalance can be compensated by introducing a large C_{DC}. Nevertheless, it is not feasible to employ large DC-link capacitors, since it adds to the volume and cost of the whole system. Therefore, compensation schemes are required in the control process to mitigate both the DC-link capacitor voltage unbalance and current distortion.

VII. Control Strategy for FSTP GSC

A. DC-Link Capacitor Voltage Deviation Suppression Control

The DC-bus voltage utilization rate is highly related to the degree of unbalance between the upper and lower DC-link capacitor voltages V_{dc1} and V_{dc2}. According to (8) and (11), the integral of phase A grid current leads to the voltage difference ΔV when neglecting the initial capacitor voltage difference. Therefore, it is feasible to eliminate the DC-bus voltage offset by subtracting a DC component in i_{ga}, and the relationship between the DC-bus voltage offset and the DC current component can be represented by a proportional gain K. The voltage deviation suppression control scheme is illustrated in Fig. 7.

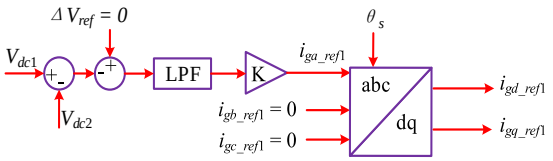


Fig. 7. DC-link capacitor voltage deviation suppression control scheme

The desired voltage deviation ΔV_{ref} is set to zero, and then the difference between ΔV_{ref} and ΔV passes through a low-pass filter (LPF) so that the high frequency components are eliminated. Then a proportional controller is applied to derive the transient DC reference value for i_{ga}. By trying different values for K, and after comprehensive consideration of both the dynamic performance and stability of the system, the proportional gain K is set as 0.16.

B. Current Distortion Compensation

In order to eliminate the distortion, capacitive impedance components can be added to phases B and C in the control process. Taking (22) to (24) into account, the reference values for v_{BO} and v_{CO} can be chosen as

$$\begin{cases} v_{BO\_ref} = \sqrt{3}ZI_m \cos(\omega_s t + \phi - \frac{\pi}{6}) + e_{gb} - e_{ga} + i_{ga} / (j\omega_s 2C_{DC}) \\ v_{CO\_ref} = \sqrt{3}ZI_m \cos(\omega_s t + \phi + \frac{\pi}{6}) + e_{gc} - e_{ga} + i_{ga} / (j\omega_s 2C_{DC}) \end{cases} \quad (25)$$

Substituting (25) into (23), and considering $i_{ga} + i_{gb} + i_{gc} = 0$, the following equations are obtained.

$$\begin{cases} i_{ga} = I_m \cos(\omega_s t + \phi) \\ i_{gb} = I_m \cos(\omega_s t + \phi - \frac{2\pi}{3}) \\ i_{gc} = I_m \cos(\omega_s t + \phi + \frac{2\pi}{3}) \end{cases} \quad (26)$$

It can be seen that the three-phase grid currents are balanced with the injection of the compensation component $i_{ga} / (j\omega_s 2C_{DC})$.

C. Overall Control Strategy

The three-phase grid voltages e_{gabc} are applied for orienting the dq reference frame, where the synchronous frequency f_{NOM} and the grid voltage angle θ_s are derived through a phase-locked loop (PLL). In order to achieve unity power factor, the reference q-axis current value is set as zero. The proposed overall control strategy for FSTP GSC in a grid-connected DFIG-WT is illustrated in Fig. 8.

The proportional and integral controller gains for the DC-bus voltage regulator are set as 0.5 and 100 respectively. For the current PI controllers, $k_{pd} = k_{pq} = 5$ and $k_{id} = k_{iq} = 500$. The derived instantaneous DC current components on the dq reference frame i_{gd_ref1} and i_{gq_ref1} are injected in the current control loop to eliminate the DC-bus voltage offset. Besides, the compensation component $i_{ga} / (j\omega_s 2C_{DC})$ is added to the reference voltages in phases B and C for the purpose of current distortion elimination.

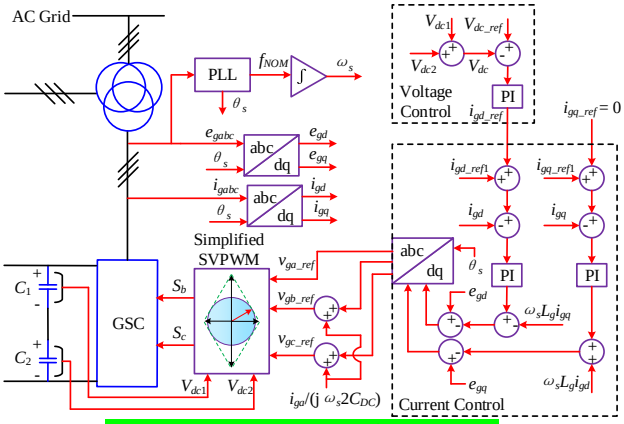


Fig. 8. Overall control strategy for FSTP GSC

VIII. Simulation Results and Discussion

The faulty scenario mentioned in previous sections is considered and the proposed simplified SVPWM technique is applied in FSTP GSC, along with the compensation schemes for DC-bus voltage balancing and phase current distortion mitigation. The supersynchronous and subsynchronous operational modes are employed for a grid-connected 1.5MW DFIG-WT with the reference rotor speeds of 1.2pu and 0.8pu, respectively. The simulations are carried out in Matlab/ Simulink2017a, and the sampling time is set as 5μs. The system parameters for the DFIG wind energy conversion system are displayed in TABLE II.

TABLE II
PARAMETERS OF DFIG-WT

Parameter	Value	Unit
Rated Apparent Power S_t	1.5	MVA
Rated Frequency F_{nom}	50	Hz
Rated Stator Voltage	575	V
Stator Resistance R_s	0.023	pu
Rotor Resistance R_r	0.016	pu
Stator Leakage Inductance L_{ls}	0.18	pu
Rotor Leakage Inductance L_{lr}	0.16	pu
Magnetizing Inductance L_m	2.9	pu
Friction Factor F	0.01	pu
Inertia Constant H	6.85	s
Pairs of Poles p	3	\
DC Bus Capacitor C_{DC}	10000	μF
Rated Wind Speed v_w	11	m/s

Two different situations are taken into account for the operation of DFIG-WT: 1) The wind speed fluctuates between 7m/s and 15m/s for the supersynchronous mode and between 7m/s and 10m/s for the subsynchronous one (Case 1); 2) Based on the scenario in Case 1, three-phase grid voltages drop to 50% of the rated values from 0.2s to 0.3s (Case 2). The wind speed fluctuation is emulated by a random input with the step time of 0.01s. In the fault-tolerant FSTP GSC, the proposed simplified SVPWM technique is employed, and different control strategies are applied. For simplicity, the control strategies of FSTP GSC without and with the proposed compensation schemes are called FSTP1 and FSTP2, respectively. From Figs. 9 to 11, the performances of SSTP and FSTP GSCs are compared, while comparison between the voltage balancing effects by applying FSTP1 and FSTP2 is carried out in Fig. 13. The three-phase grid total output currents are illustrated in Fig. 9 for SSTP and FSTP GSC topologies for both the two operational modes.

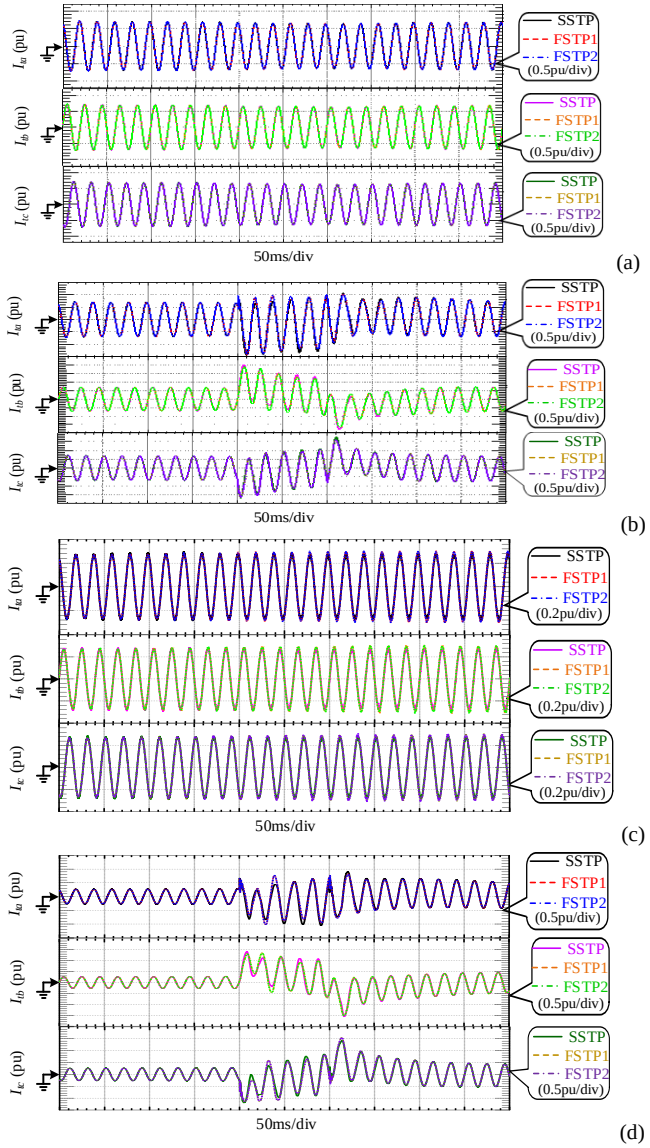


Fig. 9. The three-phase total output currents i_{tabc} for (a) Case 1 and (b) Case 2 for the supersynchronous mode and (c) Case 1 and (d) Case 2 for the subsynchronous mode

It can be seen from Fig. 9(a) and (c) that almost sinusoidal three-phase grid total output current waveforms are maintained for Case 1 by using either the SSTP or FSTP GSC. After the grid voltage sag is introduced, as is shown in Fig. 9(b) and (d), oscillations of the three-phase currents are presented during the low voltage period. In addition, the current waveforms return to the normal states around 0.5s after the low voltage period for each control strategy. Therefore, the performance of three-phase output currents by

applying FSTP GSC with the proposed SVPWM technique is almost identical to that by applying the normal SSTP GSC. To further investigate the feasibility of the proposed SVPWM technique and compensation schemes, Fast Fourier Transformation (FFT) analysis is carried out to calculate the magnitudes of harmonic components. The results of FFT analysis are displayed in TABLE III and TABLE IV for the supersynchronous and subsynchronous operational modes, respectively.

TABLE III
FFT ANALYSIS OF CURRENT HARMONIC COMPONENTS FOR THE SUPERSYNCHRONOUS OPERATIONAL MODE

Magnitude of Fundamental(50Hz) Component/THD	Case 1	Case 2
SSTP Phase A	0.7257/1.29%	0.7257/1.29%
SSTP Phase B	0.7281/1.42%	0.7281/1.42%
SSTP Phase C	0.7271/1.27%	0.7271/1.27%
FSTP1 Phase A	0.7294/1.02%	0.7294/1.02%
FSTP1 Phase B	0.7309/1.33%	0.7309/1.33%
FSTP1 Phase C	0.7305/1.67%	0.7305/1.67%
FSTP2 Phase A	0.7324/0.87%	0.7324/0.87%
FSTP2 Phase B	0.7334/1.49%	0.7334/1.49%
FSTP2 Phase C	0.7308/1.60%	0.7308/1.60%

TABLE IV
FFT ANALYSIS OF CURRENT HARMONIC COMPONENTS FOR THE SUBSYNCHRONOUS OPERATIONAL MODE

Magnitude of Fundamental(50Hz) Component/THD	Case 1	Case 2
SSTP Phase A	0.1832/5.86%	0.1832/5.86%
SSTP Phase B	0.1845/5.14%	0.1845/5.14%
SSTP Phase C	0.1828/5.11%	0.1828/5.11%
FSTP1 Phase A	0.1878/3%	0.1878/3%
FSTP1 Phase B	0.1869/5.76%	0.1869/5.76%
FSTP1 Phase C	0.187/4.97%	0.187/4.97%
FSTP2 Phase A	0.1839/3.23%	0.1839/3.23%
FSTP2 Phase B	0.1883/5.34%	0.1883/5.34%
FSTP2 Phase C	0.1869/5.37%	0.1869/5.37%

According to TABLE III and TABLE IV, the statistics in Case 1 and Case 2 are totally the same for the currents in three phases, which means that the grid voltage sag has no effect on the harmonic components. After the GSC reconfiguration is made from SSTP to FSTP, the THD in i_{ta} and that in i_{tb} are slightly reduced, while it is achieved at the expense of deteriorating the current quality of i_{tc} for the supersynchronous case. When the DFIG-WT operates in the subsynchronous mode, obvious reduction in the THD of i_{ta} is presented. Besides, there is no obvious current waveform distortion in the other two phases.

Apart from guaranteeing high output current quality, the GSC is also responsible for keeping the DC-bus voltage stable and regulating the output power factor. The simulation results of the important variables to be considered in DFIG-WT are illustrated for SSTP, FSTP1 and FSTP2 in Fig. 10 and Fig. 11 regarding Cases 1 and 2 respectively.

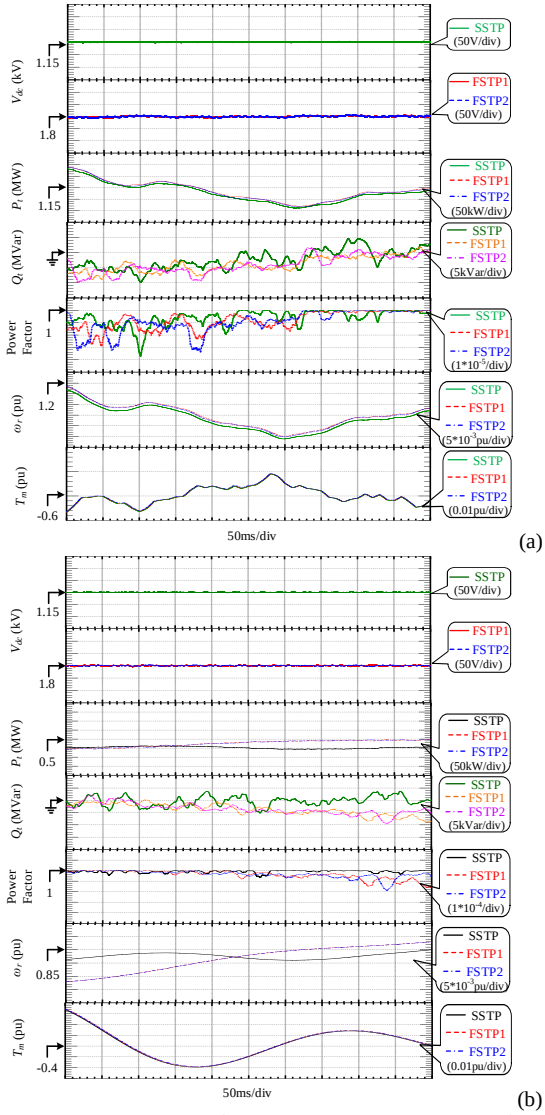
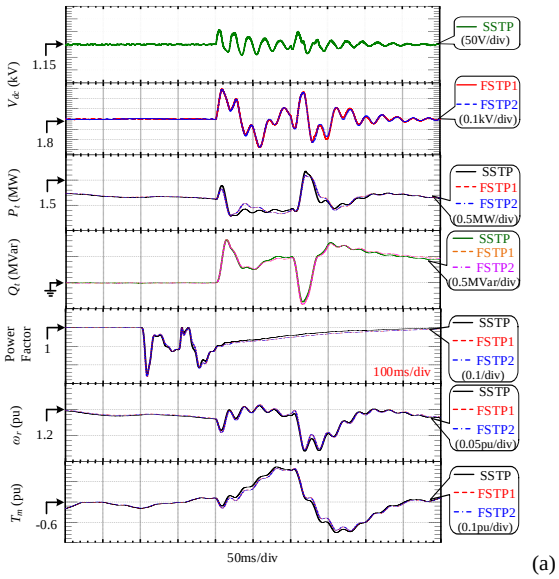


Fig. 10. Simulation results for important variables in Case 1 for (a) supersynchronous mode and (b) subsynchronous mode



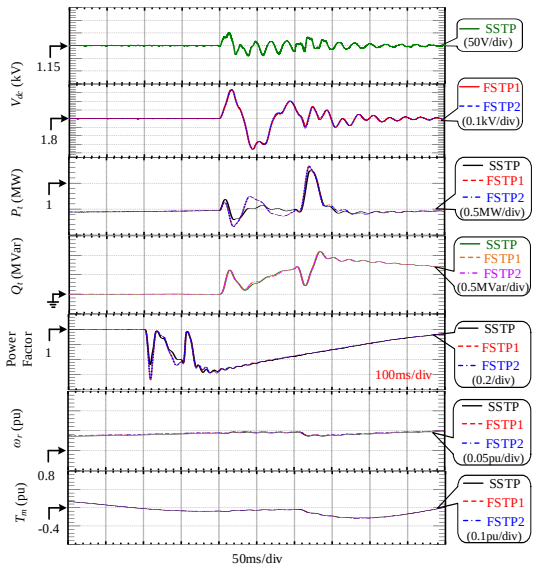


Fig. 11. Simulation results for important variables in Case 2 for (a) supersynchronous mode and (b) subsynchronous mode

From Fig. 10, the DC-bus voltage rises from 1.15kV to 1.8kV after GSC reconfiguration, which is smaller than the theoretical value of 2.3kV to mitigate the damage to DC-link capacitors. In addition, unity output power factor is maintained, which verifies that the proposed SVPWM technique and compensation schemes are applicable for FSTP GSC when the wind speed fluctuates regularly. In Fig. 11, the grid voltage drops to 0.5pu is considered during 0.2s to 0.3s, and the power factor decreases from at the beginning of the voltage sag for both operational modes. In addition, significant fluctuations in the total output reactive power Q_t can be observed, while it started approaching 0 instantly after the low voltage period. Moreover, since fewer switches are employed for the FSTP GSC topology, the switching losses are reduced. To sum up, the performance of FSTP GSC is nearly the same as that of the SSTP one.

In order to verify the DC-bus voltage tracking ability when the control strategy changes, the open-circuit fault is assumed to happen at 0.1s and the fault-tolerant FSTP control strategy is applied immediately. The tracking of the DC-bus voltage for both the two cases is illustrated in Fig. 12.

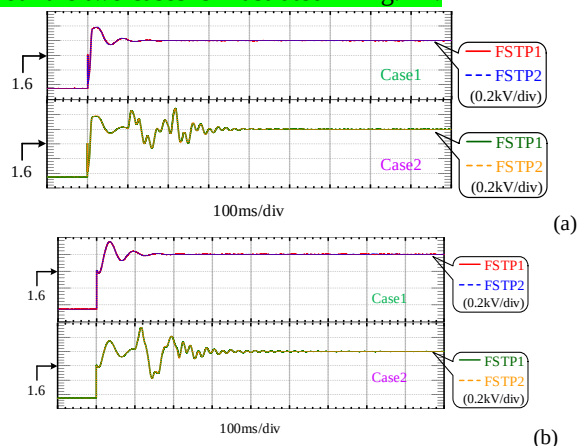


Fig. 12. DC-bus voltage step change for (a) the supersynchronous mode and (b) the subsynchronous mode

From Fig. 12, it can be observed that in both operational modes, the DC-bus voltage can track the reference value precisely after the change of control strategy. Besides, serious fluctuations terminate at around 0.4s. With the proposed voltage deviation compensation strategy, the DC component in the capacitor voltage difference is to be suppressed, and the simulation results are displayed in Fig. 13.

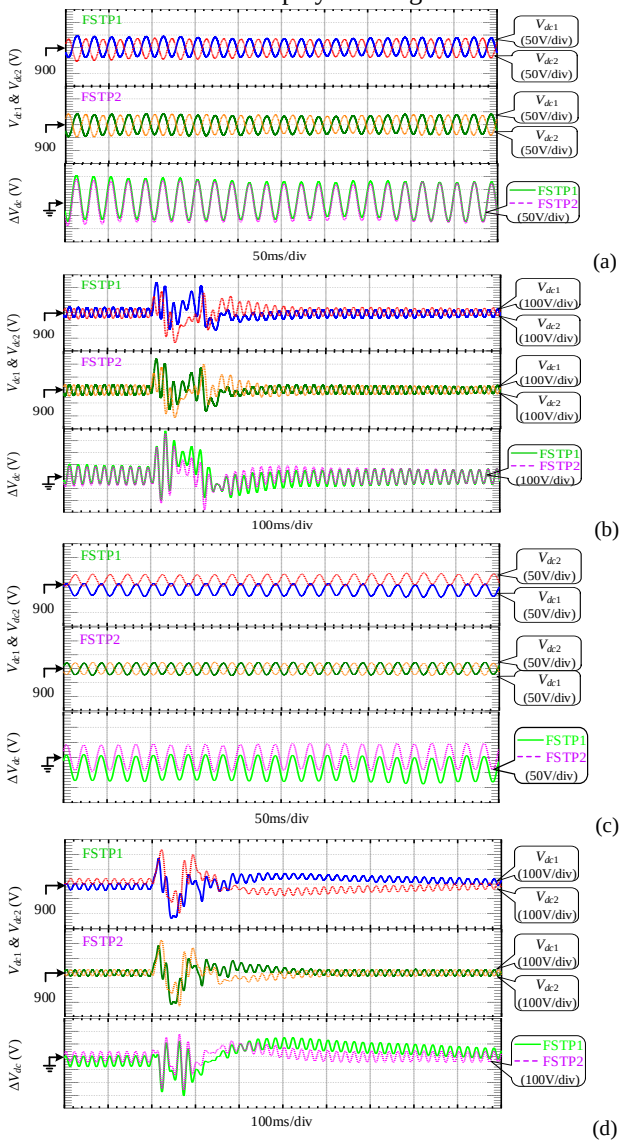


Fig. 13. Voltage balancing for (a) Case 1 and (b) Case 2 for the supersynchronous mode and (c) Case 1 and (d) Case 2 for the subsynchronous mode

From Fig. 13, it can be seen that by applying FSTP2, the average value of ΔV_{dc} over the whole period approaches zero. In Case 1, the largest instantaneous voltage differences for FSTP1 and FSTP2 are approximately 100V and 90V respectively for the supersynchronous mode, and they are approximately 80V and 40V respectively for the subsynchronous mode. In Case 2, the instantaneous voltage difference between V_{dc1} and V_{dc2} by employing FSTP1 is larger than that by employing FSTP2 in most of the time,

especially for the subsynchronous mode. Furthermore, when the proposed compensation scheme is applied, the average value of voltage deviation returns back to 0V more swiftly. Therefore, the overall performance of FSTP GSC based DFIG-WT can be improved and the damage to DC-link capacitors can be mitigated by employing the proposed compensation scheme.

IX. Conclusion

This paper studied an FSTP GSC for post-fault operation of DFIG-WT. A simplified SVPWM technique is proposed to improve the overall output current quality of the three-phase grid total output currents and reduce the computational burden. On top of that, a DC-bus voltage deviation suppression scheme is proposed to balance the DC-link capacitor voltages. Furthermore, the phase current distortion is analysed from the AC point of view for FSTP GSC, and the compensation scheme is explained. According to the simulation results by applying the proposed control strategy for FSTP GSC in two different cases:

a) Lower switching losses are derived.

b) Almost sinusoidal output current waveforms are obtained.

c) Unity output power factor can still be achieved.

d) The upper and lower DC-bus voltages are well balanced.

Overall, continuous operation of faulty grid-connected DFIG-WT can be accomplished by applying the proposed SVPWM technique and compensation schemes in FSTP GSC, even when wind speed fluctuations and grid voltage sags are included.

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